PATENT
Attorney Docket No.: 100204840-1
Facsimile Number: (571) 273-2885

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Wayne Dervon Kever, et al.	Confirmation No.:	6616
Serial No.:	10/681,815	Group No.:	2825
Filed:	October 8, 2003	Examiner:	Sun J. Lin
For:	Systems And Processes For Asymmetrically Shrinking a VLSI Layout		

Mail Stop Issue Fee
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Sir:

The Examiner has cited reasons for allowance in this application in connection with the Notice of Allowance mailed January 27, 2006. It appears the Examiner's reasons for allowance do not recite the exact language of the claims. We wish to point out that the exact language of these claims is the best recitation supporting the reasons for allowance.

Further, Applicants wish to point out that there are additional reasons for allowance, including features of independent and dependent claims not specifically referenced in the Notice of Allowance.

Also, Applicants note the Examiner cites Claims 1-28 are allowed. Applicants believe this was a typographical error and should read Claims 1-18.

Respectfully submitted,

By: _____

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